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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/801,676

03/17/2004

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EXAMINER

OVEISSI, DAVID M

ART UNIT

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2616

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PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/801,676	<b>Applicant(s)</b> ANDRE GENDARME ET AL.	
	<b>Examiner</b> David Oveissi	<b>Art Unit</b> 2616	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)            | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____                                      |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>17 March 2004</u> .   | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Claim Objection***

1. The phrase "adapted to" recited in claim 1 lines 12-13, claim 2 line 18, claim 3 line 25, and claim 4 line 30 are not positively recited claim limitation MPEP 2111.04. Therefore, the limitations after the phrase are not considered the claims limitation. It is suggested applicant to remove the phrase.

### ***Claim Rejections - 35 USC § 103***

2. This application currently names joint inventors. In considering patentability of claims under 35 U.S.C. 103(a), examiner presumes that subject matter of various claims was commonly owned at time any inventions covered herein were made absent any evidence to contrary. Applicant is advised of obligation under 37 CFR 1.56 to point out inventor and invention dates of each claim that was not commonly owned at time a later invention was made in order for examiner to consider applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining scope and contents of prior art.
2. Ascertaining differences between prior art and claims at issue.
3. Resolving level of ordinary skill in pertinent art.
4. Considering objective evidence present in application indicating obviousness or nonobviousness.

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4. Following is a quotation of 35 U.S.C. 103(a) which forms basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though invention is not identically disclosed or described as set forth in section 102 of this title, if differences between subject matter sought to be patented and prior art are such that subject matter as a whole would have been obvious at time invention was made to a person having ordinary skill in art to which said subject matter pertains. Patentability shall not be negated by manner in which invention was made.

Claims 1-7 are rejected under 35 U.S.C 103(a) as being unpatentable over **Anastas et al. (US 4,328,542)** in view of **Chen et al. (US 2001/0030950 A1)**.

For claim 1 **Anastas** a telecommunication device including a plurality of processors (P1-P4) interconnected with a plurality of memories (M1-M6) (*see Fig.3 column 10 lines 22*).

**Anastas** also teach memories and processors are *characterized* in that the plurality of processors (P1-P4) and the plurality of memories (M1-M6) are respectively arranged as an input/output border column and an input/output border row of an interconnecting matrix architecture, the matrix architecture being constituted by a plurality of interconnection devices (I<sub>11</sub>- I<sub>46</sub>) adapted to interconnect the processors of the column with the memories of the row (*see Fig.3 column 10 lines 22*). **Anastas** does teach a Digital Subscriber Line (DSL) telecommunication device) with a first path for transferring data in a first direction and a second path for transferring data in a second direction opposite to the first direction. Furthermore, **Chen** from the same field of endeavor

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teaches this limitation (*see abstract, paragraphs 50*). Thus, it would have been obvious to the person of ordinary skill in the art at the time of invention to combine the memory-processor system of **Anastas** with the DSL system of Chen. The motivation for this combination is to provide better performance and fault tolerance.

For claim 2 **Anastas** teach a Digital Subscriber Line telecommunication device, characterized in that the telecommunication device further includes control circuits adapted to control the interconnection devices ( $I_{11}$ -  $I_{46}$ ) for establishing and releasing connections between predetermined processors (P1-P4) and predetermined memories (M1 -M6) (*see column 14 lines 45-68*).

For claim 3 **Anastas** teach a Digital Subscriber Line telecommunication device, characterized in that the control circuits are further adapted to control the interconnection devices ( $I_{11}$ -  $I_{46}$ ) to establish either read access or write access or both to the memories (*see abstract and Fig. 2 and Fig. 8*).

For claim 4 **Anastas** teach a Digital Subscriber Line telecommunication device, characterized in that each interconnection device of the plurality of interconnection devices is adapted to connect a particular processor of the plurality of processors with a particular memory of the plurality of memories(*see Fig.3 column 10 lines 22*).

For claim 5 **Chen** teaches teach a Digital Subscriber Line telecommunication

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device, characterized in that the first path is a downstream path and in that the second path is an upstream path (*see paragraph 50*).

For claim **6 Chen** teaches teach a Digital Subscriber Line telecommunication device, characterized in that the telecommunication device operates according to the Very High Speed Digital Subscriber Line [VDSL] protocol (*see paragraph 63*).

For claim **7 Anastas** teaches a method for optimizing the transfer of data between memories (M1-M6) and processors (P1-P4) of a Digital Subscriber Line [DSL] telecommunication device (*see column 2 lines 41-62*),

characterized in that the memories (M1-M6) are shared by the processors (P1-P4), each processor being able to read data from or to write data to any of the memories under control of control circuits (*see column 10 lines 15 -20*).

5. Claims **8-10** are rejected under 35 U.S.C 103(a) as being unpatentable over **Anastas et al. (US 4,328,542)**, in view of **Chen et al. (US 2001/0030950 A1)** further in view of **Pincus et al. (US 6,282,583 B1)**.

For claim **8 Anastas** and **Chen** teach all aspect of the invention with the exception of a method, characterized in that a processor may simultaneously access one or more memories during a same predetermined period of time (t3, t4). However,

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**Pincus** from the same field of endeavor teaches this limitation (*see column 2 lines 1-2 and lines 60-63*). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the inventions to combine the teaching **Pincus** with **Chen** and **Anastas**. The motivation for this combination is better use of the bandwidth.

For claim **9** **Anastas** and **Chen** teach all aspect of the invention with the exception of a method, characterized in that, when during a the period of time (t3) a first processor (P1) needs to access a first memory (M2) already accessed by a second processor (P2) during the period of time (t3), the access of the first processor is delayed until a next period of time (t4). However, **Pincus** from the same field of endeavor teaches this limitation (*see column 2 lines 1-2 and lines 60-63 and Fig. 10 "144"*). Thus, it would have been obvious to the person of ordinary skill in the art at the time of the inventions to combine the teaching **Pincus** with **Chen** and **Anastas**. The motivation for this combination is better use of the bandwidth.

For claim **10** **Anastas** and **Chen** teach all aspect of the invention with the exception of a method according, characterized in that a predetermined number of successive periods of time (t1-t4) are arranged in a frame (T1, T2, T3), and in that the frame is cyclically repeated. However, **Pincus** from the same field of endeavor teaches this limitation (*see column 2 lines 1-2 and lines 60-63 and Fig. 10 "144", "168", and "170"*). Thus, it would have been obvious to the person of ordinary skill in the art at the

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time of the inventions to combine the teaching **Pincus** with **Chen** and **Anastas**. The motivation for this combination is better use of the bandwidth.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These are **Hillis (5,008,815)**, **Dietrich, Jr. et al. (5,457,789)**, and **Albal et al. (4,949,338)**.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Oveissi whose telephone number is (571) 270-3127. The examiner can normally be reached on Monday to Friday 8:00 AM to 5:00 PM EST.

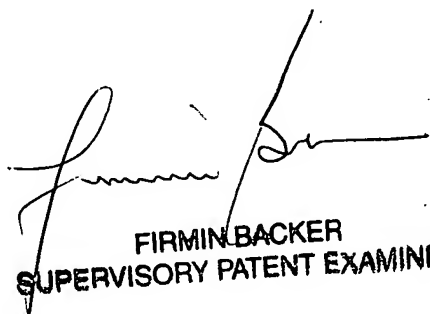
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Backer Firmin can be reached on (571) 272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

D.O



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SUPERVISORY PATENT EXAMINER